OV7610 SINGLE-CHIP CMOS VGA COLOR DIGITAL CAMERA
OV7110 SINGLE-CHIP CMOS VGA B&W DIGITAL CAMERA

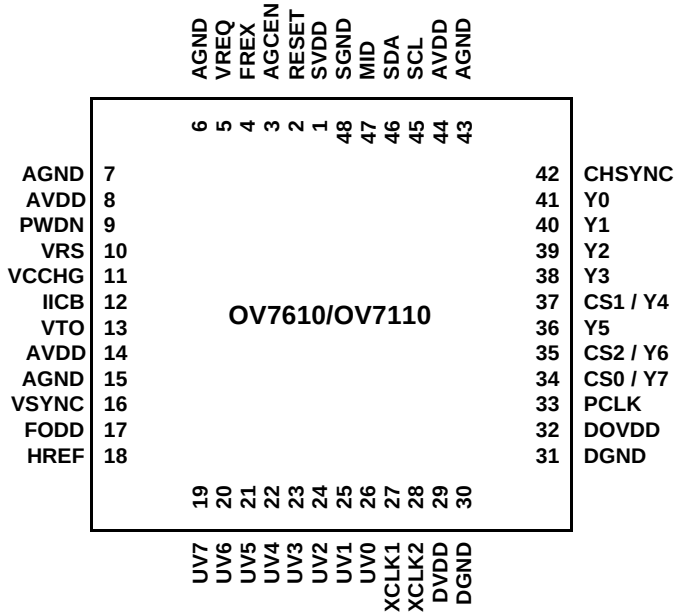
Features

- **307,200 pixels, 1/3" lens, VGA / CIF format**
- **Read out - progressive / Interlace**
- **Data format - YCrCb 4:2:2, GRB 4:2:2, RGB Original**
- **8/16 bit video data: CCIR601, CCIR656, ZV port**
- **Video Timing - 525 line, 30 fps**
- **Wide dynamic range, anti-blooming, zero smearing**
- **High-speed I^2C interface**
- **Electronic exposure / Gain / white balance control**
- **Image enhancement - brightness, contrast, gamma, saturation, sharpness, window, etc.**
- **Internal / external synchronization scheme**
- **Frame exposure / line exposure option**
- **5 Volt operation, low power dissipation.**

General Description

The OV7610/OV7110 is a single chip digital color video camera device. It incorporates a 640 x 480 image array, which is capable of operating up to 60Hz interlace or 30Hz progressive. Based on the proprietary sensor technology, inside the chip, FPN is fully cancelled, smear is eliminated and blooming is drastically reduced. All camera functions, such as exposure, gamma, gain, white balance, color matrix, windowing, are programmable through I^2C interface. OV7110 is the uncolored version for monochrome application.

- **Video Conferencing**
- **Video Phone**
- **Video Mail**
- **Still Image**
- **PC Multimedia**



OV7610/OV7110 Pin Out Diagram

Array Elements	644 x 484
Pixel Size	8.4 x 8.4 um
Image Area	5.4 x 4 mm
Electronic Exposure	500 : 1
Scan Mode	progressive interlace
Gamma Correction	0.45/1.0
Minimum Illumination	OV7610 -2.5 lux @ f1.4 OV7110 -0.5 lux @ f1.4 (3000K)
S/N Ratio (Digital Camera Out)	> 48 dB (AGC = Off, Gamma = 1)
Power Supply	5VDC, ±5%
Power Requirements	<200mW Active <100uW Standby
Package	48-pin LCC

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BG Version 1.3, 15 May 1999

1. Pin Assignment

Table 1. Pin Descriptions (Pin Type and Default Level:I-1: digital input+100k pull up, I-0: digital input+100k pull down, XI/XO: xtal IO, /S: function set during power up.O/I: digital CMOS level output Bias: power supply bias

Pin #	Name	Class	Function
1	SVDD	Bias	Sensing Power (+5V) pins.
8, 14,44	AVDD	Bias	Analog Power (+5V) pins.
29	DVDD	Bias	Digital Power (+5V) pins.
32	DOVDD	Bias	Digital I/O Power (+5V / +3.3V) pins.
48	SGND	Bias	Sensing ground connections. Connect to supply common
6, 7, 15, 43	AGND	Bias	Analog ground connections. Connect to supply common
30, 31	DGND	Bias	Digital ground connections. Connect to supply common
2	RESET	I-0	Chip reset, “high” active.
3	AGCEN	I-0	AGCEN =1 enables the Auto Gain Control. AGCEN = 0 disables it. This pin setting is effective when pin IICB = 1.
4	FREX	I-0	Frame exposure control input, effective in progressive scan only. The positive width of FREX defines the exposure time.
5	VrEQ	1.2V	Internal voltage reference. Requires an 0.1uF decoupling capacitor to ground.
9	PWDN	I-0	PWDN =1 puts chip in power down (sleep) mode.
10	**VrS**	4.0V	Internal voltage reference.
11	VcCHG	2.5V	Internal voltage reference. Requires a 1uF decoupling capacitor to ground.
12	IICB	I-0	IICB = 1 selects the power-up method of programming the internal functions. IICB = 0 selects the I^2C internal register programming method. Results of the power-up method can only be changed by a new power-up or reset sequence.
16	VSYNC	O/I	Vertical sync output. This pin is asserted high during several scan lines in the vertical sync period.
17	FODD	O	Odd field flag. Asserted high during the odd field, low during the even field.
18	HREF	O/I	Horizontal window reference output. HREF is high during the active pixel window, otherwise low.
19–26	UV[7:0]	O/I	Digital output UV bus. These pins are used for 16-bit operation for outputting chrominance data.
27, 28	XCLK1, XCLK2	XO, XI	XCLK1 and XCLK2 are the input/output of the on-chip video oscillator. Nominal crystal clock frequency is 27MHz. If an external clock is used, input to XCLK1, leave XCLK2 unconnected.
33	PCLK	O	Pixel clock output. By default, data is updated at the falling edge of PCLK and is stable at its rising edge. PCLK runs at the pixel rate in 16-bit bus operations and twice the pixel rate in 8-bit bus operations.
34–41	Y[7:0]	O/I	Digital output Y bus. In a 16-bit operation, the luminance data is clocked out of this bus at the rate of one byte per pixel. In 8-bit operation, the luminance data and the chrominance data is multiplexed to this bus.
34	CS0 (shared with Y7)	I-0/S	ID configuration bit for the I^2C slave ID.
35	CS2 (shared with Y6)	I-0/S	ID configuration bit for the I^2C slave ID.
37	CS1 (shared with Y4)	I-0/S	ID configuration bit for the I^2C slave ID.
42	CHSYNC	O	Digital output for either composite sync or horizontal sync signal.
45	SCL	I	I^2C Serial clock input with schmitt trigger.
46	SDA	O/I	I^2C Serial data, output is open-drain, input with schmitt trigger.
47	MID	I-0	Multiple I^2C slave ID enable. MID = 1 I^2C slave ID is configurable through power up setting in CS(2:0) MID = 0 I^2C slave ID is preset to 42H/43H.

2. Functional Description

The OV7610/OV7110, shown in Figure 1., Block Diagram, consists of a 1/3-inch VGA format color imaging array, the analog processing, timing controls, I^2C register controls, dual A/Ds, and digital output port. The output data type is selectable between YCrCb and RGB. Its array supports either VGA or CIF image size. The digital output format is supports standards such as CCIR601 16bit, CCIR601 8 bit, ZV Port and CCIR656.

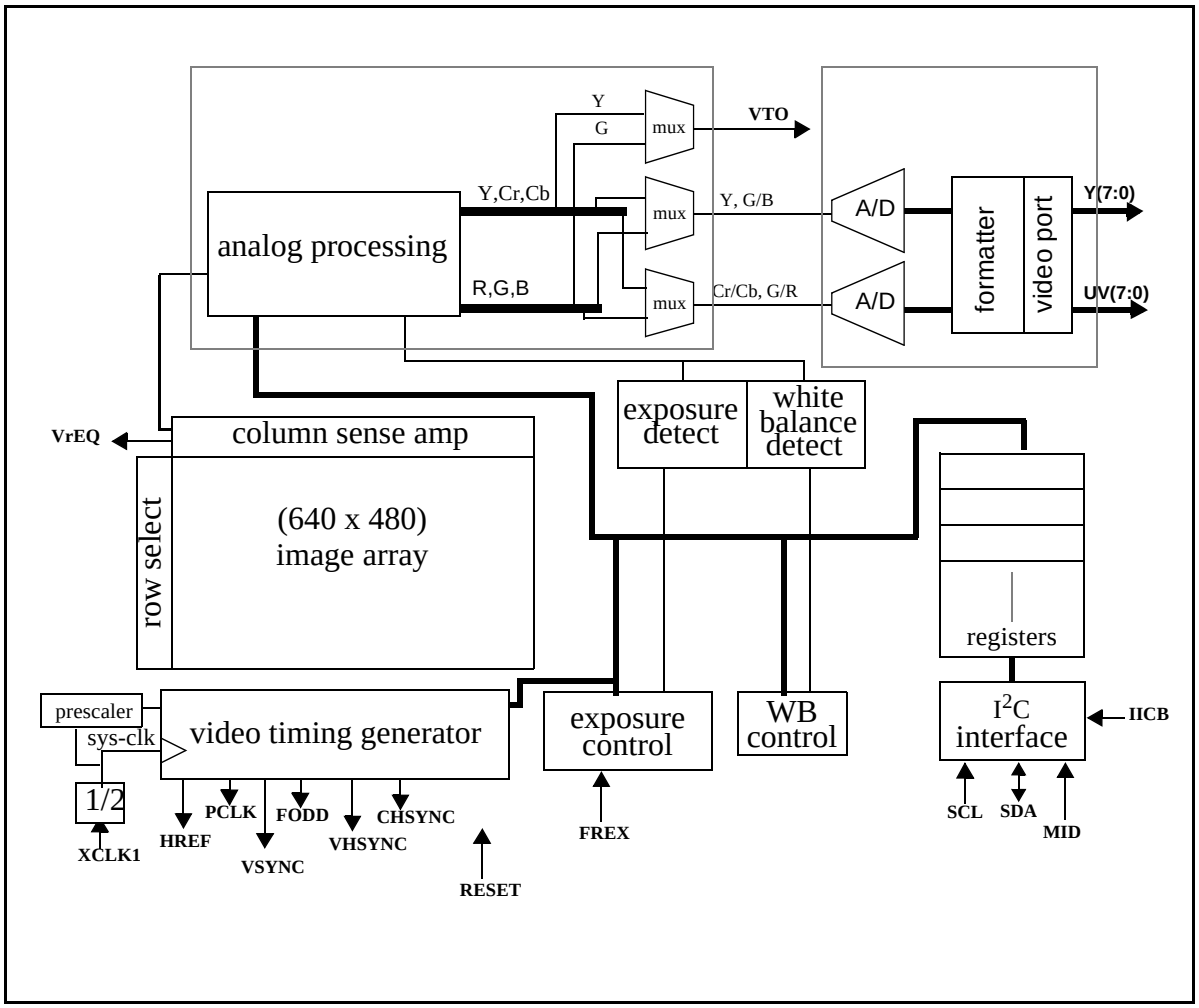

Figure 1. Block Diagram

2.1 Image Data Type

OV7610/OV7110 supports four image data type: **monochrome**, **raw color pixel**, **YUV422**, and **GBR422**.

The monochrome array is the raw color array before colorations. The raw color array adopts primary Bayer color pattern GR/BG as in Figure 2., Raw Color Array. Two built-in color space converters map the raw color array to RGB image planes and YUV image planes as shown in Figure 3., Video Image Mapping (644x484). Y and G planes are each VGA size, U,V and R,B are each half VGA size. OV7610/OV7110 can output either original pixel data, the YUV plane or the RGB planes. In either one, the default image size is 640x480 pixels, the maximum image size is 644x484 pixels.

Two ways to obtain the CIF (320x240) image size, one uses the internal subsampling scheme which reduces the full image to 1/4 size, the other uses window function to crop 1/4 portion of the full image.

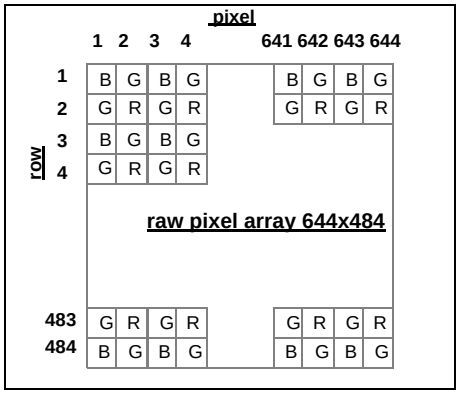

Figure 2. Raw Color Array

2.2 Bus Standards

OV7610 uses two closely tied 8 bit video buses (Y channel and UV channel) to deliver video stream.

In dual channel operation, which includes standards CCIR601-16bit 422, ZV-PORT and straight 16bit data out of A/D, Y channel is either Y image plane data, G image plane data, or Odd line raw pixel data. UV channel is either UV image plane data, RB image plane data, or Even line raw pixel data.

In single channel operation, which includes standards CCIR601-8bit 422, CCIR656 422 and straight 8bit data out of A/D, Y channel is multiplexed data stream taken either from Y/U/V image planes, R/G/B image planes or raw pixel array.

The data format for dual channels is:

YUV422-
- YYYY...
- UVUV...

Raw color array -
- GRGR...
- BGBG...

GBR422 -
- GGGG...
- BRBR...

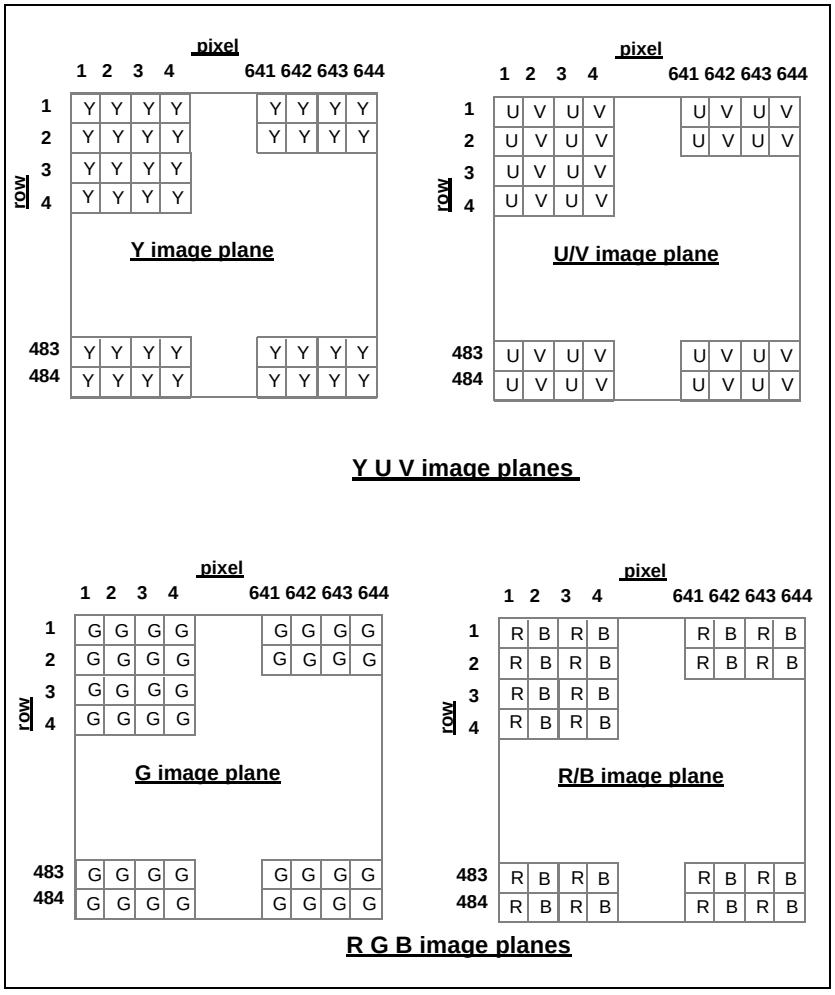

Figure 3. Video Image Mapping (644x484)

2.3 Scan Method

The timing of this device is based on 525 line 60Hz TV standard. There are up to 480 active scan lines in an image. OV7610/OV7110 can operate in either interlace scan or progressive scan. Interlace scan reads 240 lines in a field, and takes two fields to complete an image frame, progressive scan reads all 480 lines in single field, i.e. each field is an image frame.

Interlace scan, odd line is read in odd field, even line is read in even field, i.e. rows 1,3,5...,479 are read in odd field, rows 2,4,6....480 are read in even field.

Progressive scan, this chip implements various read out schemes to support all image maps.

For Y/UV or RGB image planes, the array is read in row order, i.e rows 1,2,3...480.

For RAW pixel array, the progressive scan has one-line scheme and two-line scheme:

One-line scheme reads one row a time, i.e. rows 1,2,3,...,480.

Two-line scheme reads two lines a time using both Y/UV channels, i.e. the row order for the (Y/UV) channels are: (2/1),(2/3),(4/3),(4/5),(6/5),(6/7)...(478/479),(480/479). * *In this case, each row is repeatedly output twice, both contains the same image information.*

2.4 Data Order

OV7610/OV7110 allows data(pixel) to be reordered, coupling with various image data types and single/dual channels output, greatly increase the chip flexibility.

For monochrome application,

BW - to route all pixels to Y channel throughout the entire signal path, the result is much balanced signal level.

For RGB application,

YG -to route all 'G' data to Y channel, all 'RB' data to UV channels. This feature takes the advantage of widely used YUV422 postprocessing scheme and apply to RGB planes to become GBR422.

Other format related features :

XUV - to swap the order of U and V in UV plane, or R and B in RB plane.

XY8 - to swap the order of Y and UV, or G and RB in single channel (8bit) operation.

W720 - to extend the image width to 720 pixels by adding 76 black pixels before the 644 regular pixels.

CIF60 - enable the same CIF image in both even/odd filed interlace scan, effectively doubles frame rate,

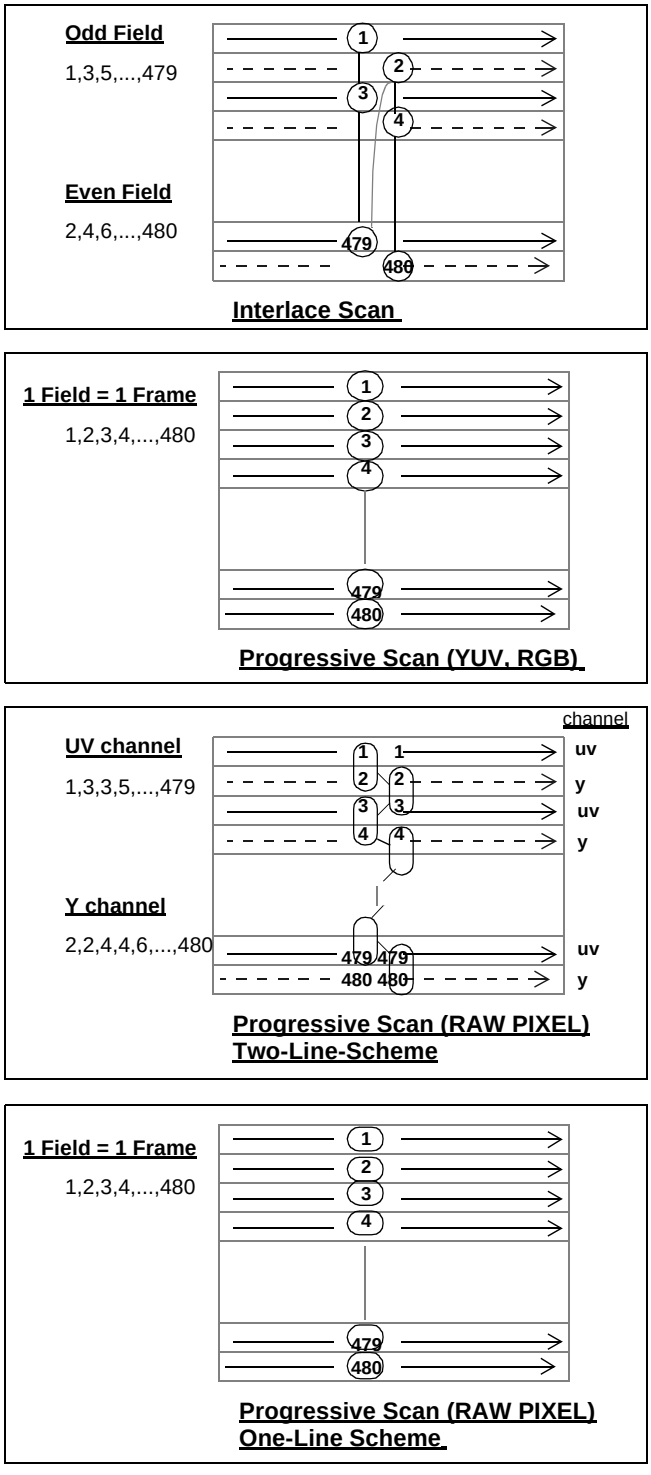

Figure 4. Scanning Schemes

The following table summarize all the available combinations.

Table 2. Data Type & Scan Mode

		Interlace			Progressive		
Resolution		**640x480**	**720x480**	**320x240**	**640x480**	**720x480**	**320x240**
YUV 4:2:2	16Bit	Y	Y	Y	Y	Y	Y
	8Bit	Y	Y	Y	Y	Y	Y
	CCIR656	Y	Y				
RGB 4:2:2	16Bit	Y	Y	Y	Y	Y	Y
	8Bit	Y	Y	Y	Y	Y	Y
	CCIR656	Y	Y				
Y/UV swap[2]	16Bit						
	8Bit	Y	Y		Y	Y	
U/V swap	YUV[3]	Y	Y		Y	Y	
	RGB	Y	Y		Y	Y	
YG	16Bit	Y	Y	Y	Y	Y	Y
	8Bit						
One Line	16Bit				Y	Y	
	8Bit						

2.5 A/D

The two on-chip 8-bit A/Ds are capable of delivering up to 13.5MS/sec. The operation is fully synchronous to the pixel rate, the actual conversion rate is determined by the clock prescaler. The operation of A/D is completely auto, which requires no user intervention.

2.6 Exposure control

The built-in auto exposure algorithm is optimized for normal scene, where the subject is well-lit compared to the background. Along with the AEC on chip, is the AGC, which can boost to its maximum gain. Since the internal AEC has a range of 500:1 (progressive) and 1:250 (interlace), for most applications, the camera's AEC can adjust itself to match the lighting condition without user intervention. AEC/AGC can be disabled, in this case, manual exposure and gain setting can be done through programming registers "Exp,Gain".

2.7 White balance & Color Temperature Correction

OV7610 maintains color consistency by channel balancing. A well balanced channels ensures image is truly white balanced. The white balance operation can be performed automatically or manually.

Individual registers are available to fine tune the ratio of red and blue components, providing a simple means to correct the color temperature.

2.8 Clock Prescaler

OV7610 includes a clock prescaler. This allows master clock to be divided down to achieve different frame rate other than the standard 60Hz under 27Mhz input clock frequency. One application is to slow down internal clock by in order to increases chip sensitivity. The other application is to adjust frame rate to match with utility power frequency in order to reduce flickering.

2.9 Windowing

The windowing feature allows users to size the window for cropping purpose. The window is sizable from 4 x 4 to 644 x 484 and can be placed anywhere inside the image boundary. Referring to window formula described in the register section.

Note: This function does not change the frame rate or data rate. It simply changes the assertion of the HREF to match the horizontal and vertical region that is programmed by the user.

2.10 Interface Support

OV7610's timing is based on standard 60Hz TV standard. The composite sync timing is available in certain package in pin CHSYNC. Odd field indicator is through pin FODD and vertical sync timing is in pin VSYNC. HREF, PCLK are required for CCIR601 and ZV-port format.

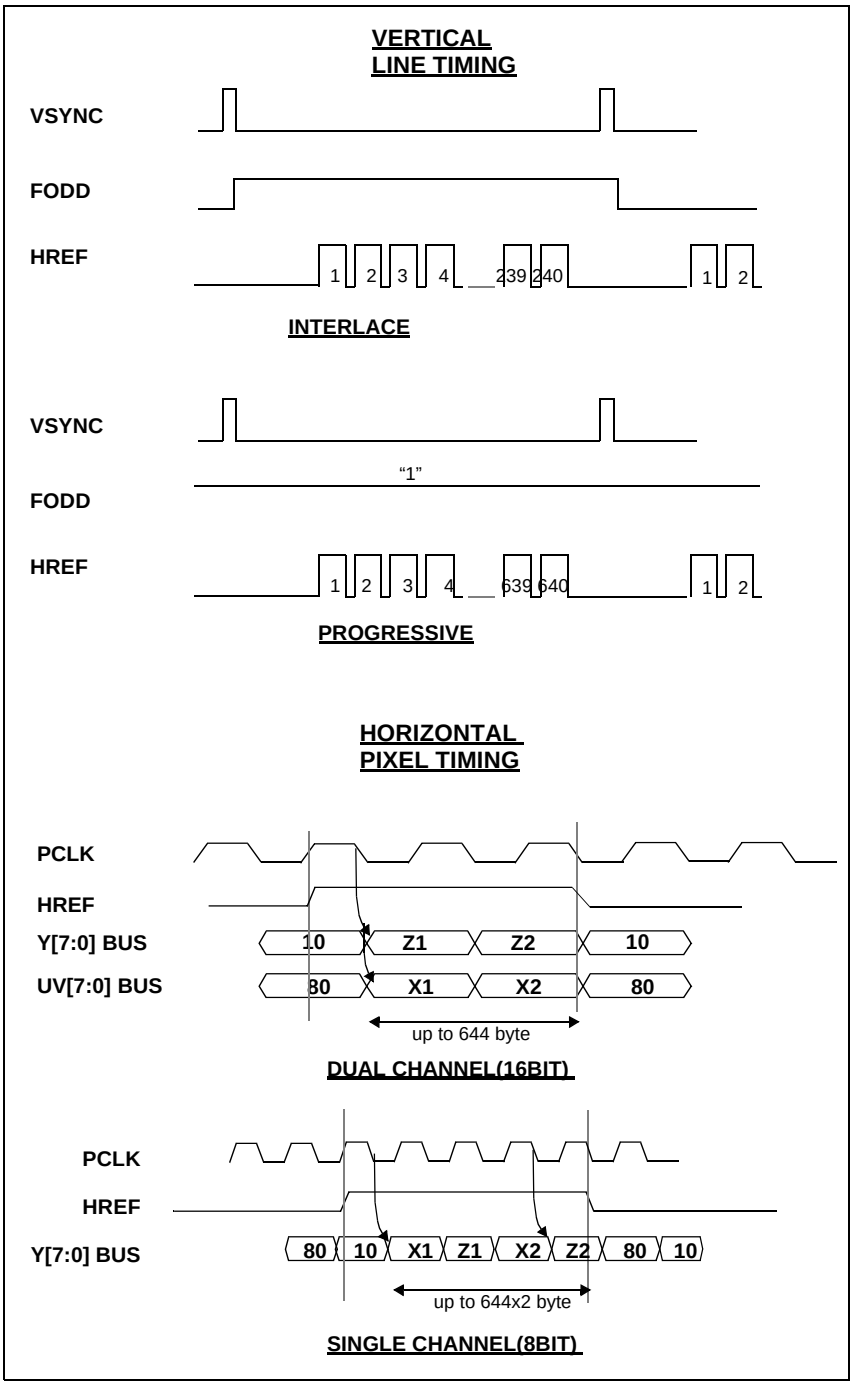

Figure 5. Video Capturing

3. External Sync Operation (Slave mode)

By default, OV7600 operates in master mode, i.e. Hsync,Vsync are outputs signals. However, this device can operates in slave mode, i.e. Hsync, Vsync are inputs. To operate, first switch to slave mode so I/O direction is switched,

External master provides: Clk, Hsync, Vsync;
Timing requirements: Hsync = 858 CLK, Vsync = 525 Hsync.
Chip outputs: PCLK, HREF.

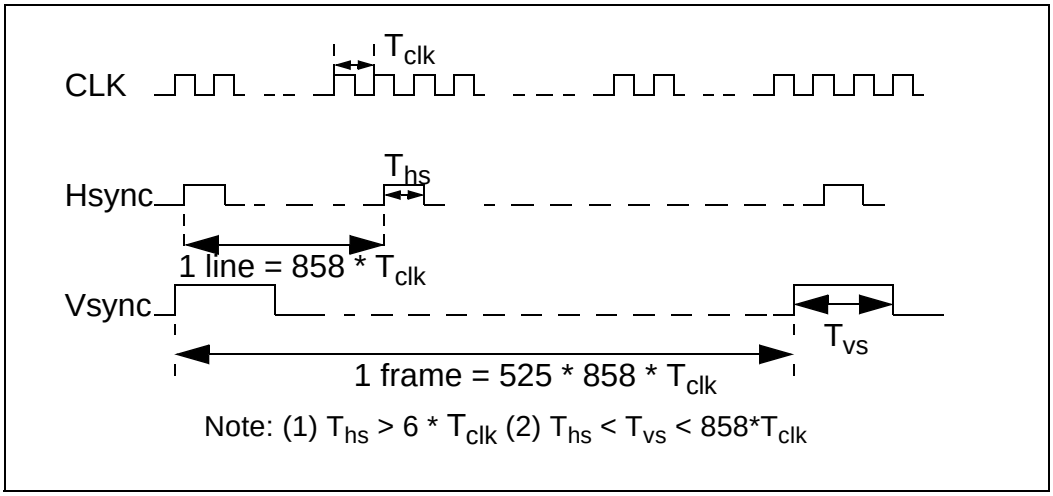

Figure 1. (Slave Mode) External Sync

4. Multiple chip Synchronize

**** Pin FSIN is replaced by RESET, therefore, this function is not accessible.***

5. Image State Output

OV7600 provides image information through Y channel, allowing external controller to implement auto exposure auto gain and auto white balance algorithm.

1. Line luminance average level - **Ylav**;
2. Field/frame luminance average level - **Yfav**;
3. Field/frame Green component average level - **Rfav**;
4. Field/frame Red component average level - **Bfav**;
5. Field/frame Blue component average level - **Gfav**.

If enabled, both line and field image information are available:

5.1 Line State

The pixel data is averaged per line and attached to the last 4 bytes of the Y channel video data within each HREF window. In case of YUV planes, the Y data is averaged. In case of RGB planes, G data is averaged.
In CIF size, the last 2 bytes contain the image information.

5.2 Field State

The line pixel information is still attached to the last 4 bytes of the HREF window. Four extra entire image averaged data, Yfav/Rfav/Bfav/Gfav, are attached to the last four lines of valid vertical window.

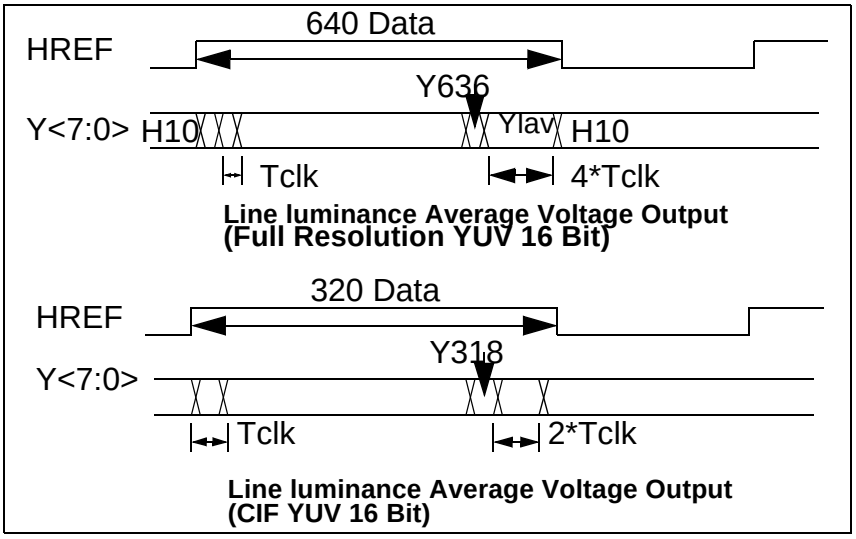

Figure 7. Line State Output

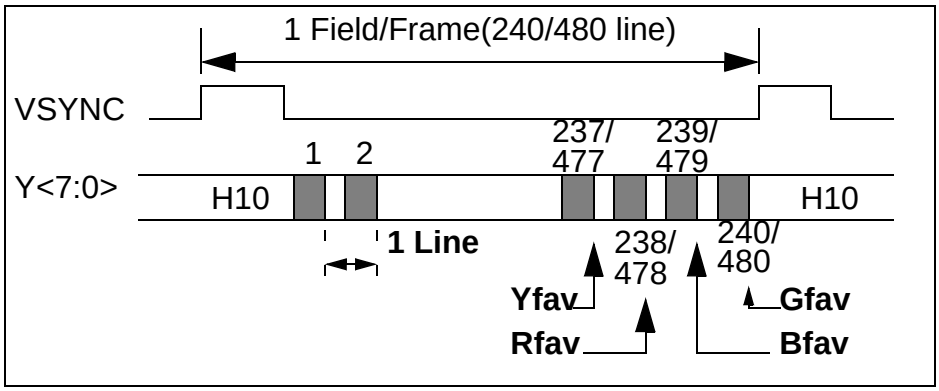

Figure 8. Field State Output

6. I²C Bus

Pin IICB = 0 selects the I²C access. The OV7610/OV7110 is an I²C slave device that supports 400 kbps, 7-bit address data transfer protocol as shown in Figure 9. on page 10.

"Restart" feature is not supported here. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte. Standard I²C requires only two pins: SCL and SDA. SDA is configured as open drain for bidirectional purpose. A HIGH to LOW transition on the SDA while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA while SCL is HIGH indicates a STOP condition. Only a master can generate START/STOP conditions. Except these two special conditions, the protocol requires SDA to be stable during the HIGH period of the clock SCL. Each bit can only change state when is SCL LOW. See Figure 10. on page 11.

6.1 I²C Bus Protocol

The I²C access is enabled only if pin IICB = 0. The OV7610/OV7110 is a slave device that supports 400 kbps, 7-bit address data transfer protocol.

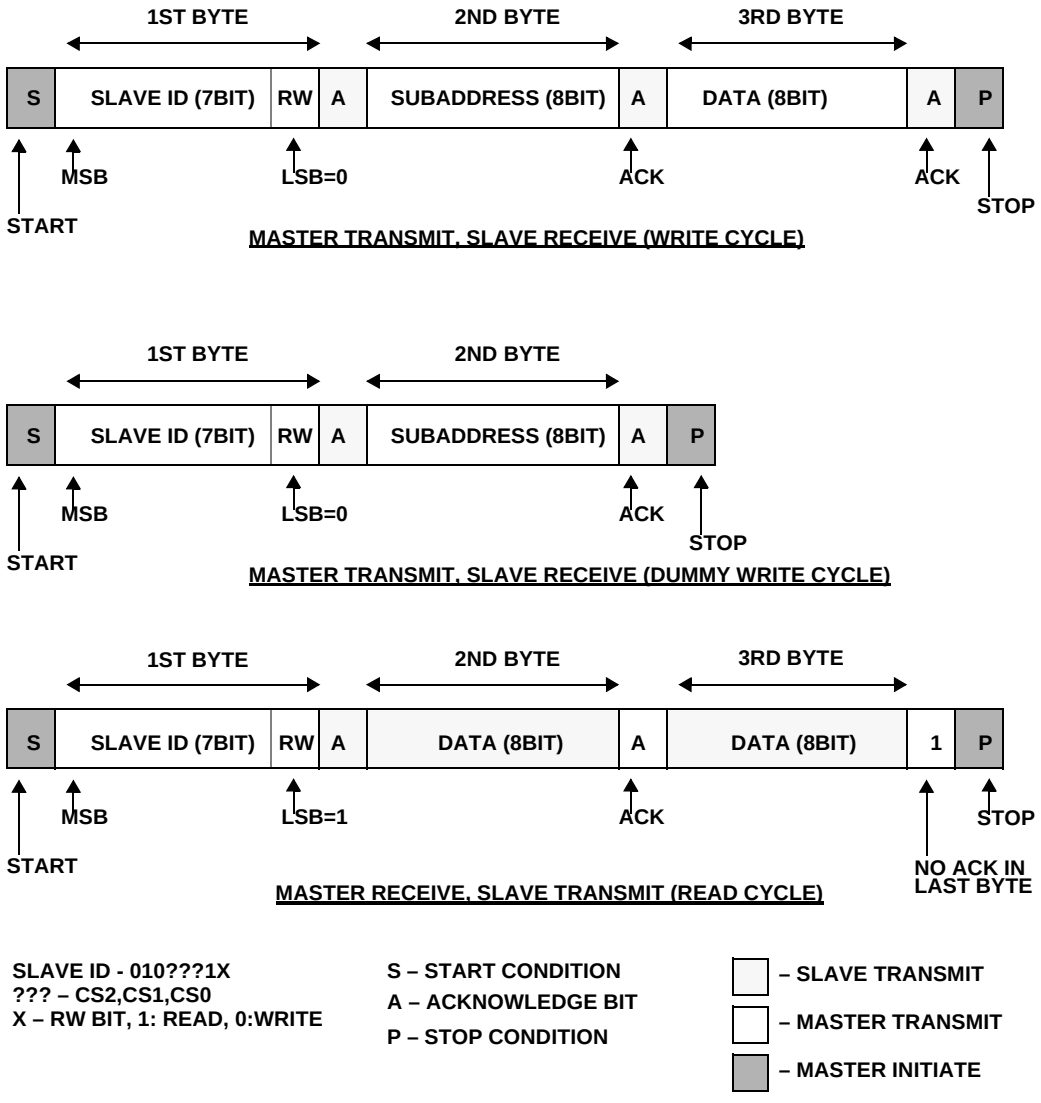

Figure 9. I²C Bus Protocol Format

Note that the restart feature is not supported here. Within each byte, MSB is always transferred first. Read/write

control bit is the LSB of the first byte. Standard I^{2}C requires only two pins: SCL and SDA. SDA is configured as open drain for bidirectional purpose.
A HIGH to LOW transition on the SDA while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA while SCL is HIGH indicates a STOP condition. Only a master can generate START/STOP conditions. Except these two special conditions, the protocol requires SDA to be stable during the HIGH period of the clock SCL. Each bit can only change state when is SCL LOW. See Figure 10. on page 11.
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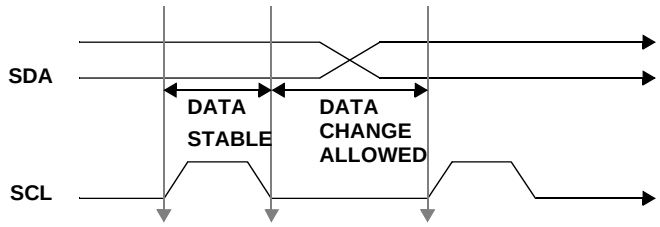


Figure 10. Bit Transfer on the I^{2}C Bus

OV7610/OV7110 reserves CS[2:0] for the slave ID configuration, which makes eight combinations. In I^{2}C operation, the master must do the following operations:

- **Generate the start/stop condition**
- **Provide the serial clock on SCL**
- **Place the 7-bit slave address, the RW bit, and the 8-bit subaddress on SDA**

The receiver must pull down SDA during the acknowledge bit time. During the write cycle, the OV7610/OV7110 returns the acknowledgment and during read cycle, the master returns the acknowledgment except when the read data is the last byte. If so, the master does not acknowledge the last data byte, so that the read cycle can be terminated.

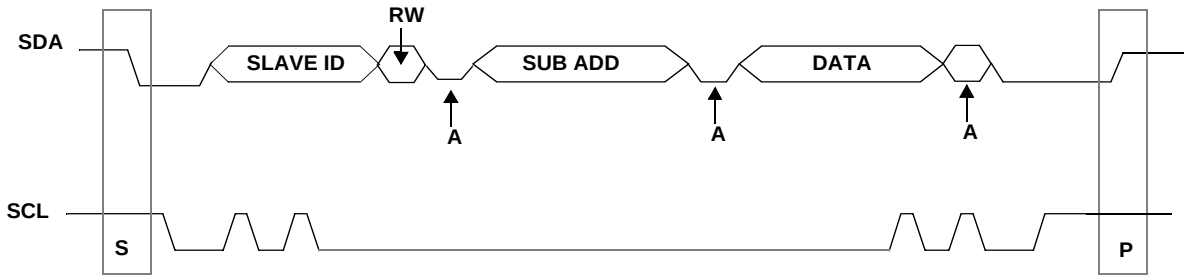


Figure 11. Data Transfer on the I^{2}C Bus

The OV7610/OV7110 I^{2}C supports multi-byte write and multi-byte read. The master must supply the subaddress. in the write cycle, but not in the read cycle. Therefore, the OV7610/OV7110 takes the read subaddress from the previous write cycle. In multi-byte write or multi-byte read cycles, the subaddress is automatically increment after the first data byte so that continuous locations can be accessed in one bus cycle. A multi-byte cycle overwrites its original subaddress; therefore, if a read cycle immediately follows a multi-byte cycle, you must insert a single byte write cycle that provides a new subaddress.
The OV7610/OV7110 supports single slave ID (pin MID=0) and multiple slave ID (pin MID=1). In single, ID is preset to 42/43. In multiple, ID is configured by setting pin CS[2:0] (high or low) to one of the eight combinations listed below at reset or power up.

Multiple Slave ID

CS[2:0]	000	001	010	011	100	101	110	111
WRITE ID(hex)	42	46	4A	4E	52	56	5A	5E
READ ID (hex)	43	47	4B	4F	53	57	5B	5F

In the write cycle, the second byte in I^2C bus is the subaddress for selecting the individual on-chip registers, and the third byte is the data associated with this register. Writing to unimplemented subaddress is ignored. In the read cycle, the second byte is the data associated with the previous stored subaddress. Reading of unimplemented sub-address returns unknown.

6.2 Register Set

Table 3. I^2C Registers

Subad-dress (hex)	Register	Default (hex)	Read/ Write	Descriptions
00	Gain[5:0]	00	RW	GC[5:0] – Gain setting. gain =(GC[5]+1)*(GC[4]+1)(GC[3:0] /16 +1) GC[7:6] - unimplemented bit, returns 'X' when read.
01	Blue[7:0]	80	RW	BLU[7:0] – blue channel balance value. "FFh"- highest, "00h"-lowest
02	Red[7:0]	80	RW	RED[7:0] – red channel balance value. "FFh"- highest, "00h"-lowest
03	Sat	80	RW	SAT[7:0] – saturation adjustment. "FFh"- highest, "00h"-lowest
04	Rsvd04	80	RW	reserved
05	Cnt	00	RW	CTR[7:0] – Y signal contrast adjustment. "FFh"-highest, "00h"-lowest
06	Brt	80	RW	BRT[7:0] – Y signal brightness adjustment. "FFh"-highest,"00h"-lowest
07	Rsvd07	D4	RW	reserved
08 - 0B	Rsvd08 ~ 0B	-	-	reserved
0C	Blue Bias	20	RW	BBS[5:0] – blue channel bias value. "3Fh"-highest, "00h"-lowest
0D	Red Bias	20	RW	RBS[5:0] – red channel bias value. "3Fh"-highest, "00h"-lowest
0E	Gamma Coeff	14	RW	GAM[7] - additional 2x gain enable GAM[6] - disable color filter compensation, in BW application, set this bit to "1" GAM[4:3] - S-AWB control 00 - 0.2 01 - 0.4 10 - 0.6 11 - 0.8 GAM[2] – "1" selects value 0.45, "0" selects value 0.5, effective when COMC[2]=1 GAM[1:0] – gamma curve fine tune. 00 - 95% 01 - 90% 10 - 85% 11 - 80%

Subad-dress (hex)	Register	Default (hex)	Read/ Write	Descriptions
0F	WB Range	A5	RW	RWB[7} - AEC method 1 RWB[6] - AEC method 2 RWB[5:4] - ALC black level 00 - 1.20v 01 - 1.26v 10 - 1.30v 11 - 1.40v RWB[3:2] - S-AWB upper level limit 00 - 70% 01 - 80% 10 - 90% 11 - 100% RWB[0:1] - S-AWB lower level limit 00 - 10% 01 - 20% 10 - 30% 11 - 40%
10	Exp	7F(I)/FF(P)	RW	EC[7:0] – Manual exposure setting. Valid range: interlace 00h~7Fh; progressive 00-FFh formula for exposure time: $T_{EXPOSURE} = T_{LINE}$ x EC[7:0]x2; where T_{LINE} = Frame Time/525. The actual time of a scan line is determined by the clock rate divider. This register is only effective when operated in manual adjust mode (COMB[0] = 0). Nevertheless, this register is always accessible through the I^2C bus. It generally takes no more than two fields for the image to reach the intended exposure after changing the setting. ***** This register must be initialized to the default value when switching between scan modes, initialization must be done in manual exposure setting.***
11	Clock	00	RW	SYN[7:6] - polarity for sync timing outputs 00: HSYNC, CHSYNC, VSYNC = "- - + " 01: HSYNC, CHSYNC, VSYNC = "- - - " 10: HSYNC, CHSYNC, VSYNC = "+ - + " 11: HSYNC, CHSYNC, VSYNC = "- + + " CLK[5:0] - system clock prescaler; formula for pixel clock rate: clock rate = CLK_input / ((CLK[5:0] + 1) * 2) The effect of the change is immediate. However, it generally takes about two fields for the image to reach the stable state.
12	Common A	24	RW	COMA[7] - "1" initiates the chip soft reset, the reset takes place after the acknowledge bit is issued, the effect is the same as powerup the chip, the chip is initialized to a default state, all registers including I^2C's contents are set to default, this bit is self cleared after the reset. COMA[6] - "1" selects mirror image. COMA[5] - "1" enables AGC, for it to take effect, COMB0 must be set. COMA[4] - "1" swaps Y/UV data in 8 Bit operation, data order YUYV... COMA[3] - "1" selects RGB image plane, "0" selects YCrCb image plane COMA[2] - "1" enables auto channel balance, for it to take effect, COMB[0] must be set. COMA[1] - "1" Color Bar Test pattern. COMA[0] - "1" select Line BLC, "0" enables field BLC.
13	Common B	01	RW	COMB[7:6] - reserved. COMB[5] - "1" enable 8 bit operation, Y bus is active, UV bus is tri-stated. COMB[4] - "1" enables CCIR656 bus operation, Y bus is active, UV bus is tri-stated. COMB[3] - selects a timing signal to pin CHSYNC; "1" is composite sync, "0" is horizontal sync. COMB[2] - "1" puts Y and UV buses in tri-state. COMB[1] - "1" initiates the single frame transfer, for this function to work, field drop mode (FD<1:0> in REG 16) must set to "OFF". See Figure 12., Single Frame Transfer Example, after this bit is set, HREF is only asserted for consecutive two fields beginning at Odd field. This bit is cleared automatically at the end of this frame. Clearing this bit in the middle of active frame has no effect to the assertion of the current HREF. COMB[0] - main auto adjust mode enable. Once enabled,Reg(00,01,02,10) are set by internal auto control, read of them returns auto set value, write is ineffective because internal control will overwrite itl.
14	Common C	04	RW	COMC[7:6] - reserved COMC[5] - "1" selects CIF (320x240) image, the image is subsampled from the full VGA frame. COMC[4] - selecting timing signal to output pin VSYNC "1" - frame sync, vertical sync is asserted in every odd field, "0"- field sync, vertical sync is asserted in every field. COMC[3] - Inverting HREF polarity COMC[2] - "1" gamma value set by GAM[2]; "0" gamma value is 1.0. COMC[1:0] - reserved

Subaddress (hex)	Register	Default (hex)	Read/ Write	Descriptions
15	Common D	01	RW	COMD[7] - reserved COMD[6] - inverting PCLK polarity, "1" - video data change on rising edge "0" - video data change on falling edge, this is the default setting. COMD[5:1] - reserved COMD[0] - exchanges U V order; "0" - V U V U... 16Bit operation, V Y U Y... 8 Bit operation; "1" - U V U V... 16Bit operation, U Y V Y... 8 Bit operation.
16	Field Divide	03	RW	FD[7:2] – Field interval selection. See Figure 13. on page 18. The feature, together with FD[1:0], divides the video signal into a programmed number of time slots in units of field, and HREF is active only in one field during the period. This function does not affect the video data or pixel rate. Only one bit can be set and the valid combinations and functions are as follows: "000001" – Divide to 2 slots. HREF is asserted every 2 fields. "000010" – Divide to 4 slots. HREF is asserted every 4 fields. "000100" – Divide to 8 slots. HREF is asserted every 8 fields. "001000" – Divide to 16 slots. HREF isasserted every16 fields. "010000" – Divide to 32 slots. HREF is asserted every 32 fields. "100000" – Divide to 64 slots. HREF is asserted every 64fields. FD[1:0]- field mode selection. Interlace scan: "00" - OFF mode; HREF is not asserted in both fields, one exception is the single fame transfer operation (see the description for the register 13) "01" - ODD mode; HREF is asserted in odd field only. "10" - EVEN mode; HREF is asserted in even field only. "11" - FRAME mode; HREF is asserted in both odd field and even field. Progressive scan: "00" - OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register 13) "01,10" - SLOT mode; HREF is asserted in frame according FD<7:2>. "11" - FRAME mode; HREF is asserted in every frame. FD<7:2> useless
17	Horizontal Window Start	38	RW	HS[7:0] - selects the starting point of HREF window, each LSB represents 4 pixels, this value is set based on an internal column counter, which consists of two ranges, the default value corresponds to the first available pixel, valid ranges:37--D5h ; HS+1< HE. See Figure 14. on page 19.
18	Horizontal Window End	03	RW	HE[7:0]- selects the ending point of HREF window.
19	Vertical Window Start	05	RW	VS[7:0] - selects the starting row of vertical window, valid range: 05h ~ F5h, VS < VE Interlace scan: each LSB represents 1 scan line in one field. Progressive scan: each LSB equals 2 scan line in one frame. In CIF (COMC5=1), it is 1 scan line. See Figure 14. on page 19.
1A	Vertical Window End	F4	RW	VE[7:0] - selects the ending row of vertical window.
1B	Pixel Shift	28	RW	PS[7:0] - to shift the output pixel timing relative to that of HREF, it physically shifts the video data output time early or late in unit of pixel clock as shown Figure 15. on page 19. This function is different from changing the size of the window as defined in registers HS & HE. The default corresponds to zero shift timing, lower value results in early pixel, higher value results in late pixel. If the amount of shift is beyond the physical image boundary, the black data will be used to filled the missing pixels. Lower than default number shifts the pixel in early(right) direction, since the lowest value is "00h", there are maximum 40 early pixels as 28h-00h = 40. Higher than default number shifts the pixel in delay(left) direction, the highest number is "FFh"; so maximum shift number is: Early: 40 pixels; Late: 216 pixels.
1C	Manufacture ID (high)	7F	R	MIDH[7:0] – Read only. Always returns '7F'.
1D	Manufacture ID (low)	A2	R	MIDL[7:0] – Read only. Always returns 'A2'.
1E	Test A	C4	-	reserved
1F	Test B	04	-	reserved

Subad-dress (hex)	Register	Default (hex)	Read/ Write	Descriptions
20	Common E	00	RW	COME7 - HREF pixel number selection. "1" - HREF include 720 PCLK and first 76 pixel data are black reference level, HE[7:0] and HS[7:0] should be kept at default value; "0" - HREF width decided by HS[7:0], HE[7:0] and COMA3=0. COME6 - reserved COME5 - Luminance "3-point average" enable COME4 - "1" aperture correction enable. Correction strength and threshold value will be decided by COMF[7:4]. "0" - Disable COME3 - S-AWB enable, effective only when COMB0=1 and COMA2=1 COME2 - AWB method selection , effective only when COMB0=1 and COMA2=1. Enable condition is set by GAM[7:5]. COME1 - AWB fast/slow mode selection. "1" - fast AWB, "0" - slow AWB. When AWB enable, COMA2=1, fast AWB (power up) then slow AWB. COME0 - Digital output driver capability. "1" High drivability for digital output. "0" low drivability.
21	Y Offset	80	RW	Y channel manual offset adjustment, effective when COMG[2]=1 YOF[7] - sign bit, "1" increase, "0" - decrease YOF[6:0] - Y channel offset
22	UOffset	80	RW	U channel manual offset adjustment, effective when COMG[2]=1 UOF[7] - sign bit, "1" increase, "0" - decrease UOF[6:0] - U channel offset value
23	Rsvd23	0A	-	reserved
24	ECW	18(I)/2E(P)	RW	Exposure white level setting for AEC. ***** Note: This register must be initialized to the default value when switching between scan modes, initialization must be done in manual exposure setting. The following equation must be satisfied to ensure stable AEC.*** **AEW[7:0] + AEB[7:0] [4D] - Interlaced;** **AEW[7:0] + AEB[7:0] [9A] - progressive**
25	ECB	3F(I)/7C(P)	RW	Exposure black level setting for AEC. ***** Note: This register must be initialized to the default value when switching between scan modes, initialization must be done in manual exposure setting. The following equation must be satisfied to ensure stable AEC.*** **AEW[7:0] + AEB[7:0] [4D] - Interlaced;** **AEW[7:0] + AEB[7:0] [9A] - progressive**
26	Common F	B2	RW	COMF[7:6]: - digital aperture correction coring level [00] - 8 mV [01] - 16 mV [10] - 32 mV [11] - 64 mV. COMF[5:4]: digital aperture correction gain [00] - 50% [01] - 100% [10] - 200% [11] - 400%. COMF3 - reserved. COMF2 - swap MSB <-> LSB, default is bit7 = MSB. COMF1 - "1" enables A/D self-calibration. COMF0 - reserved.
27	Common G	C2	RW	COMG[7:4] - reserved COMG[3] - reserved COMG[2] - "1" disable Y & U & V auto offset adjustment, Y or U or V offset can be manually set in Reg21 and Reg22 and Reg2E. COMG[1] - "1" disable CCIR601 range clip, data range extends to 01h ~ FEh. COMG[0] - reserved
28	Common H	00	RW	COMH[7] - enable one-line output, valid in progressive scan COMH[6] - enable BW feature. COMH[5] - enable progressive scan COMH[4] - stop AEC/AGC, camera retains the last exposure/gain values. COMH[3] - stop AGC, camera retains the last gain value. COMH[2] - enable YG feature. COMH[1] - enable a fixed 2x gain in addition to the AGC control COMH[0] - higer AGC, "1" extends the AGC upper limit by 2x
29	Common I	03	RW	COMI[7] - stop AEC, camera retains the last exposure value. COMI[6] - enable external sync (slave) mode, hsync,vsync becomes input. COMI[5:4] - reserved COMI[3] - "1" center exposure algorithm, "0" - area exposure algorithm COMI[2] - reserved COMI[1:0] - version ID, read only

Subad-dress (hex)	Register	Default (hex)	Read/ Write	Descriptions
2A	Frame Rate H	04	RW	EHSH7 - Frame Rate adjustment enable bit. "1" Enable. EHSH<6:5> - Highest 2 bit of frame rate adjust control byte. see explanation below. EHSH4 - "1" - UV component delay 2 pixel. " 0" no 2*Tp delay. EHSH3 - Y channel brightness adjustment enable. When COMF2=1 active. EHSH2 - Always "1" EHSH1 - Always "0" EHSH0 - Always "0"
2B	Frame Rate L	00	RW	EHSL<7:0> - Lowest 8 bit of frame rate adjust control byte. Frame rate adjustment resolution is 0.12%. Control byte is 10 bit. Every LSB equal decrease frame rate 0.12%. Range is 0.12% - 112%. IF frame rate adjustment enable, COME7 must set to "0".
2C	ALC	88	RW	EXBK[7:4] - Auto Level Control high level comparator selection.Range is 0.08% - 1.3% EXBK[3:0] - Auto Level Control step selection. Range is 0.08% - 1.3%.
2D	Common J	33	RW	COMJ7 - AEC update rate selection, “1” slow , “0” faster . COMJ6 - CIF 60 frame/s selection. "1" Only Odd field in Interlace Mode data output, "0" Odd/ Even field data output, frame rate is 30 Frame/s. COMJ5 - ALC update rate selection. “1” slow, “0” fast. COMJ4 - Enable Auto Level Control. COMJ3 - reserved COMJ2 - Band filter enable. After adjust frame rate to match indoor light frequency, this bit enable a different exposure algorithm to remove light band seen under fluorescent light. COMJ1 - Always "1". COMJ0 - Always "1".
2E	VOffset	80	RW	V channel manual offset adjustment, effective when COMG[2]=1 VOF[7] - sign bit, “1” increase, “0” - decrease VOF[6:0] - V channel offset value
2F	Array Bias	30	RW	Array bias adjustment, use factory setting only
30	Rsvd30	71	RW	reserved
31	Rsvd31	90	RW	reserved
32	Rsvd32	56	RW	reserved
33	YGAMMA	A0	RW	YGAM[7] : GAMMA switch for better color resolution YGAM[6]: YGAMMA enable YGAM[5:0]: reserved
34	Bias Adjust	4A	RW	BADJ[7:6] : A/D reference level adjustment. [00] - 110% internal full signal range; [01] - 120%, [10] - 130%, [11] - 140%. BADJ[5:4]: UV low-pass-filter bandwidth selection. [00] - 0.4MHz, [01] - 0.8 MHz, [10] - 1.2MHz, [11] - 1.6 MHz. BADJ[3:2]: signal peak level adjustment. [00] - 60% of full range, [01] - 70%, [10] - 80%, [11] - 90% of full range. BADJ[1:0]: GAMMA curve selection (knee voltage) [00] - 0.9v, [01] - 1.0v, [10] - 1.1v, [11] - 1.2V
35	Common L	5E	RW	COML[7:5] - Y channel delay time selection relative to UV channel COML[4] - enable UV Filter 1 COML[3] - enable UV Filter 2 COML[2] - Y signal algorithm selections . COML[1] - Always "1". COML[0] - reserved.
36	Rsvd36		RW	reserved
37	Rsvd37		RW	reserved
38	Common K	81	RW	COMK7 - HREF edge selection w.r.t PCLK “1” - PCLK falling edge "0" - PCLK rising edge. COMK6 - High driveability for digital output pin. COMK5 - reserved. COMK4 - ZV port Vertical timing selection. "1" VSYNC output ZV port vertical sync signal. "0" normal TV vertical sync signal. COMK3 - Quick stable mode when camera mode change. (CIF, 8 Bit output, CCIR 656 mode and Progressive Scan Mode). After relative control bit set, the first VS will be the stable image with suitable AEC/AWB setting. "0" - slow mode, after mode change need more field/ frame to get stable AEC/AWB setting image. COMK2 - reserved. COMK1 - AWB settle time selection for slow AWB operation. "1" - fast “0” - slow. COMK0 - Always "1"

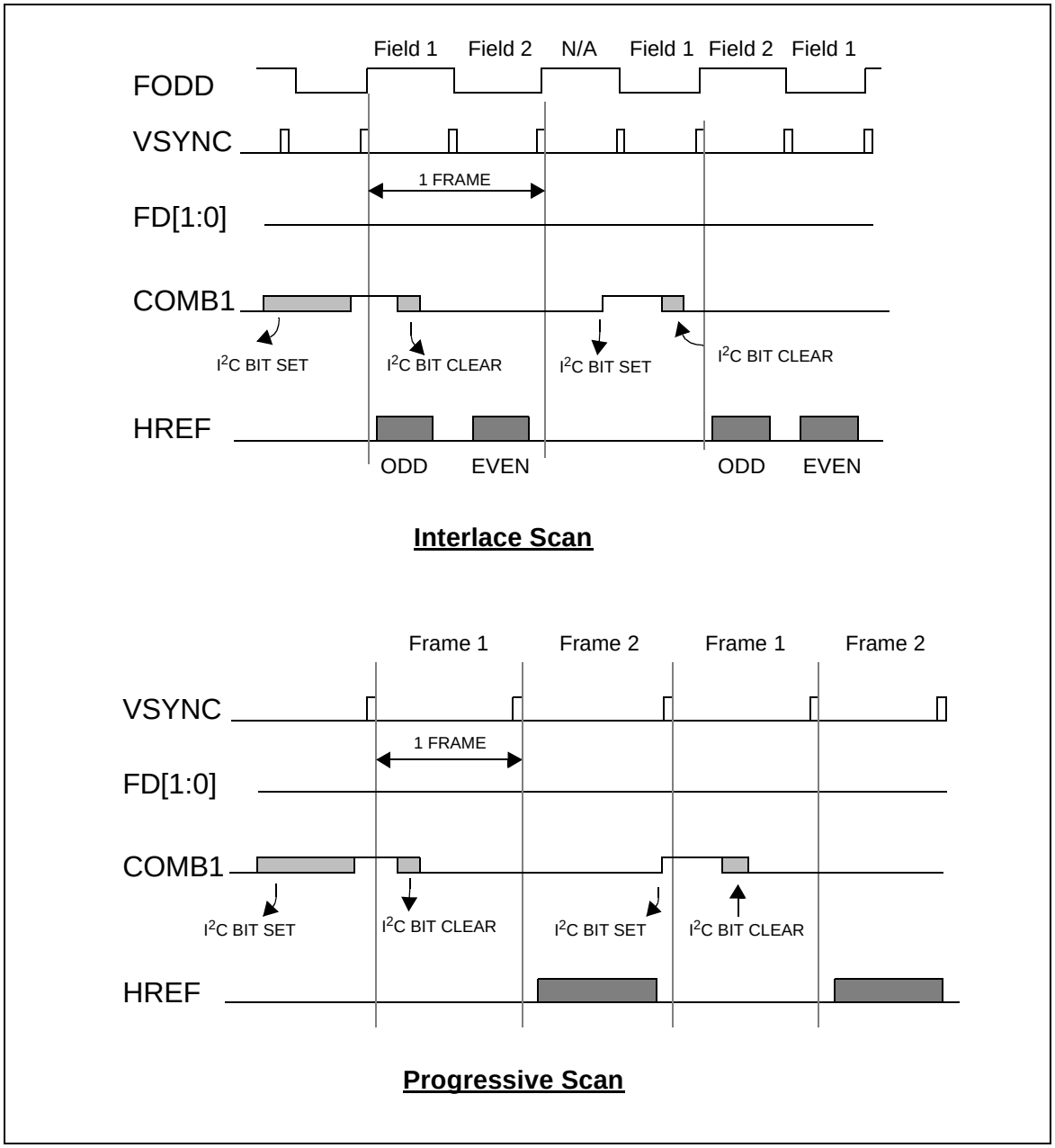


Figure 12. Single Frame Transfer Example

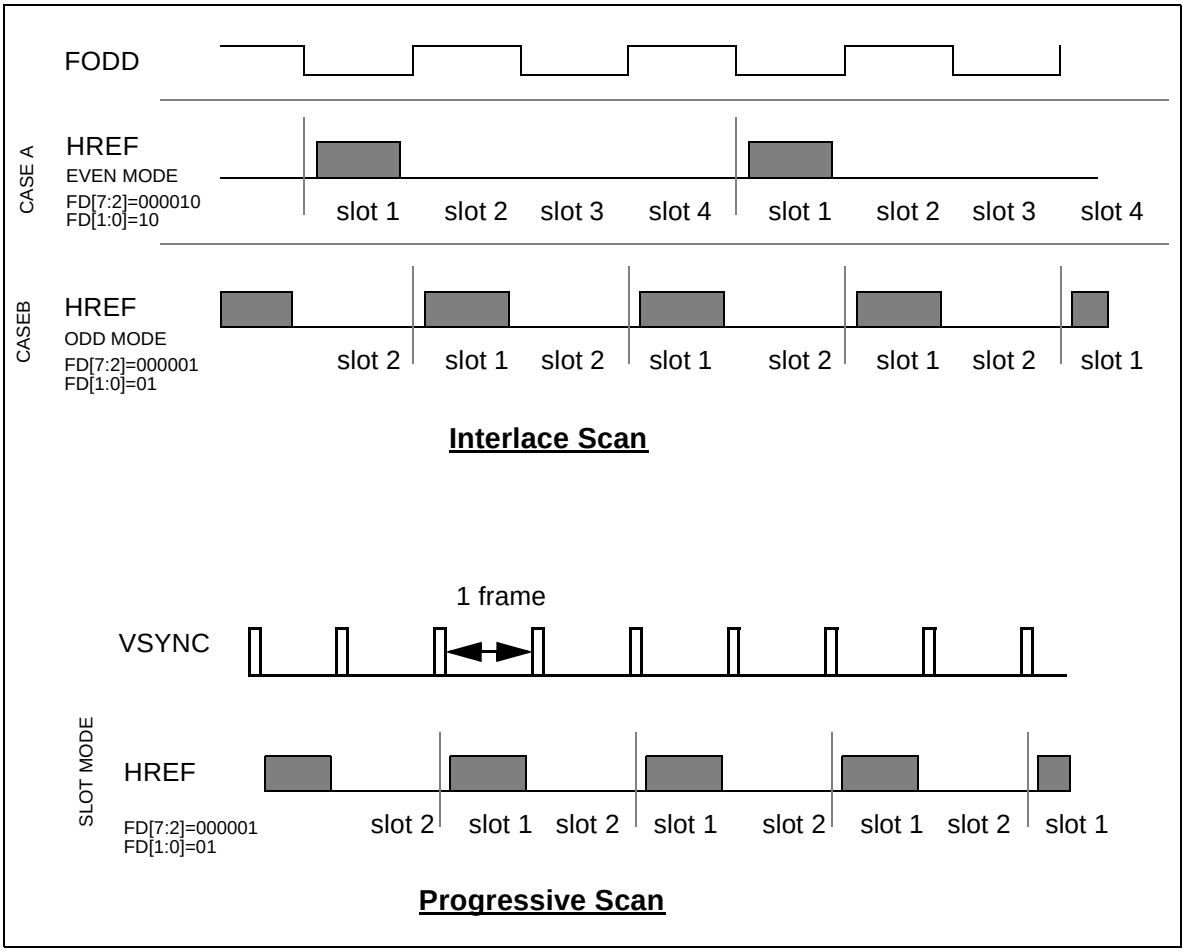


Figure 13. Field Division Example

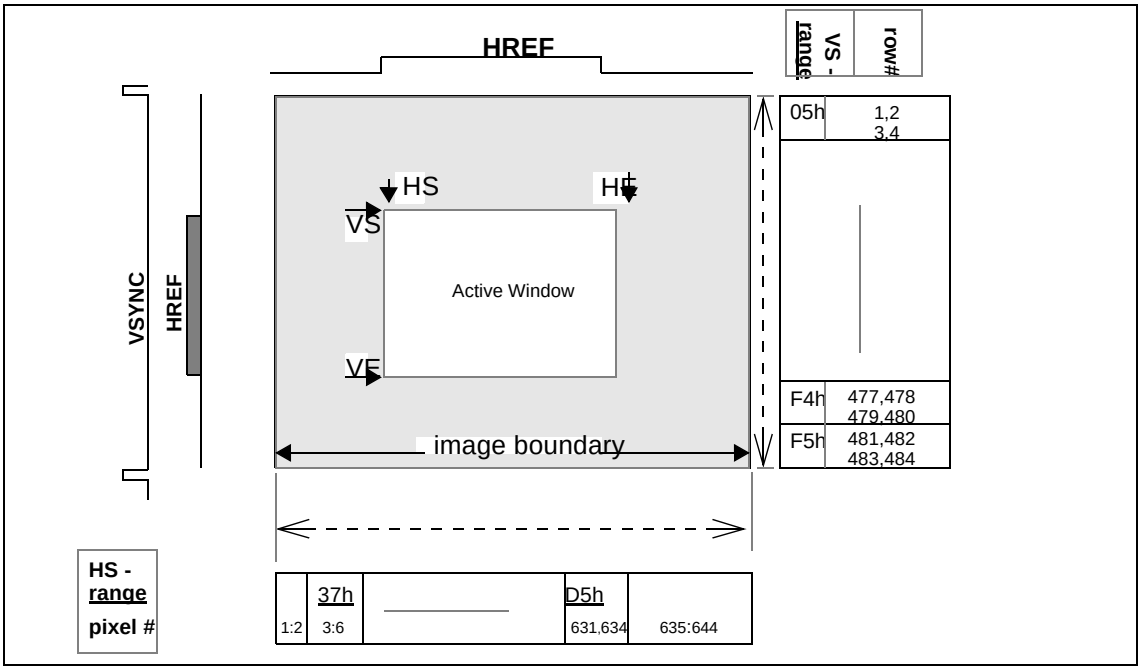


Figure 14. Window Sizing

Note 1. Valid End value must be "higher than "Start value for both VE/VS and HE/HS. At minimum, (VE-VS)=1 equals 4 rows, (HE-HS)=1 equals 4 pixels. Horizontal counter has two region, the counter wraps back to 00h after reaching D6h.

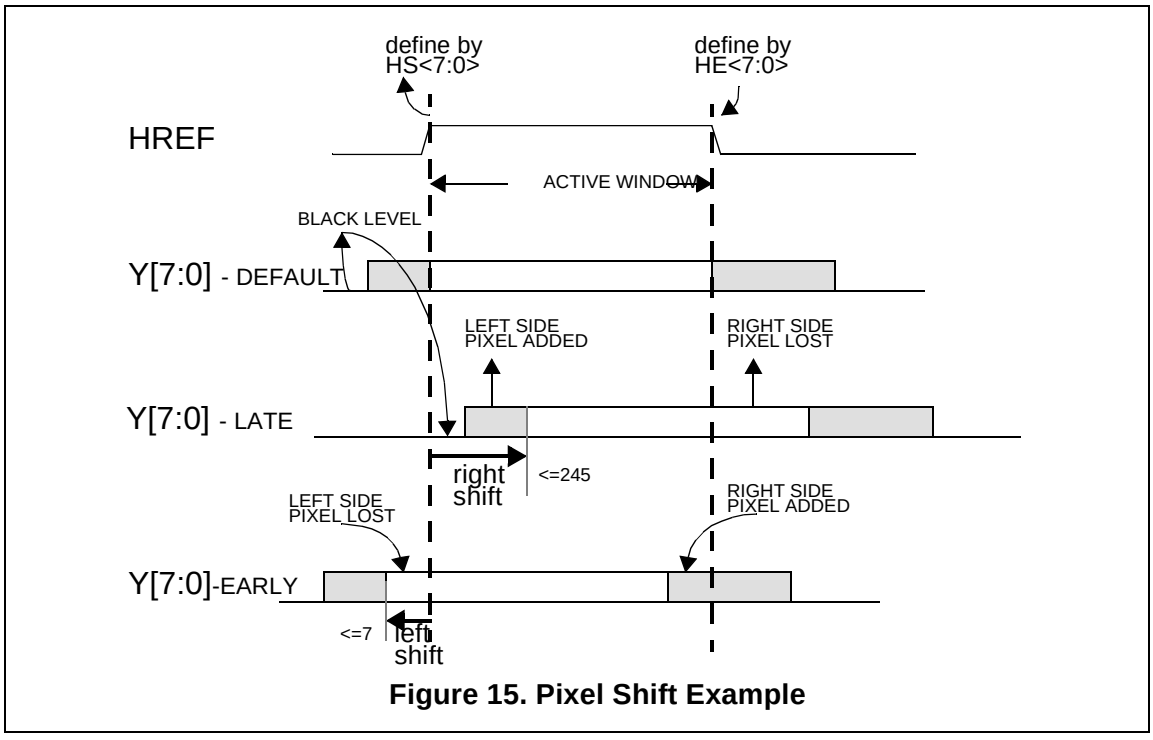


Figure 15. Pixel Shift Example

Note: pixel shift feature does not affect the order of video data in Y and UV bus.

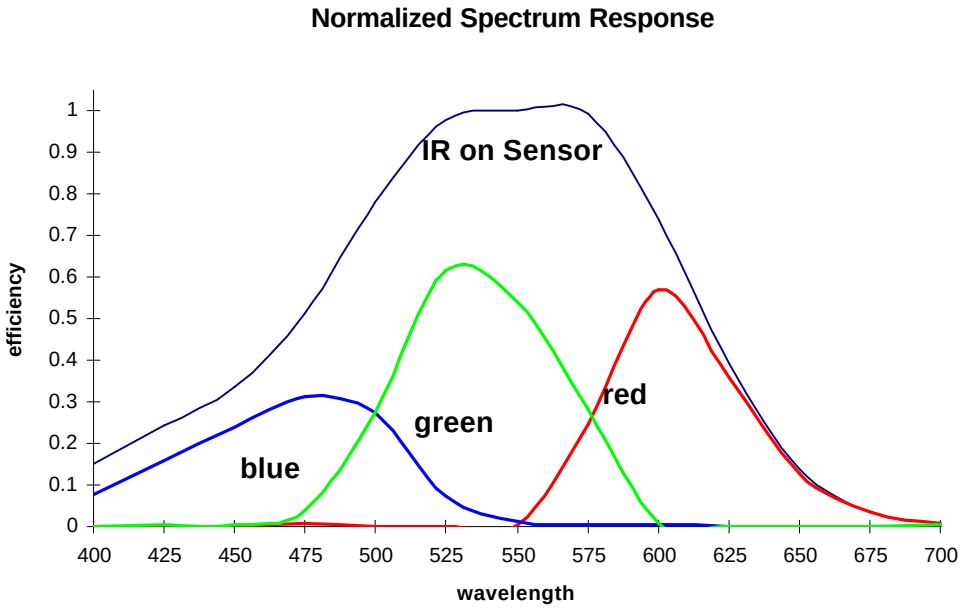
7. Specifications

Table 4. Electrical parameters (0°C to 70 °C, all voltages referenced to GND)

Symbol	Descriptions	Max	Typical	Min	Units
Supply					
V_{DD}	Supply voltage (VDD, DVDD)	5.5	5.0	4.5	V
V_{DDO}	Supply voltage (DOVDD)	5.5	-	3	V
I_{DD1}	Supply Current in VDDs	25	-	-	mA
I_{DD2}	Supply Current in DOVDD @ 50pf load at digital output	-	40	-	mA
I_{DD3}	Standby supply current (CMOS level @ inputs)	100	-	-	uA
Digital input pin					
V_{IL}	Input voltage LOW	0.8	-	-	V
V_{IH}	Input voltage HIGH	-	-	2.0	V
Cin	Input capacitor	10	-	-	pF
t_r, t_r	Digital input rise/fall time	25	-	-	ns
Digital output - standard load 50pf, 1.2kΩ to 3.0volts					
V_{OH}	Output voltage HIGH	-	-	2.4	V
V_{OL}	Output voltage LOW	0.6	-	-	V
Video bus - (@ 60Hz fps)					
t_{PCLK}	PCLK cycle time	-	74	-	ns
t_P	PCLK pulse width	-	32	-	ns
t_{DS}	data to PCLK set up time	-	t_P - 10	-	ns
t_{DH}	data to PCLK hold time	-	t_P - 10	-	ns
I^2C					
f_{scl}	SCL clock frequency	400	-	-	kHz
t_f	SDA fall time	300	-	20 + 0.1C_{sda}	ns
t_{idle}	Bus idle time	-	-	1.3	us
t_{hdsta}	START hole time	-	-	0.6	us
t_{stps}	STOP set up time	-	-	0.6	us
t_{ds}	SDA set up time	-	-	100	us
t_{dh}	SDA hold time	-	-	0	us
Clock input / Crystal Oscillator					
f_{osc}	Resonator frequency	3	27.000	30	MHz
	Load capacitor	-	10	-	pF
	Parallel resistance		1M		W
	Rise/fall time for external clock input	-	5	-	ns
	Duty cycle for external clock input	60		40	%
Misc. timing					
t_{SYNC}	External FSI cycle time	-	2	-	frame
t_{PU}	Chip power up time	100	-	-	us
t_{PD}	Power up delay time	-	10	-	us
t_{PZ}	Power up low-z delay	-	1000	-	ns
VTO analog video output parameters					

Table 4. Electrical parameters (0°C to 70 °C, all voltages referenced to GND) (Continued)

Symbol	Descriptions	Max	Typical	Min	Units
V_{TO-P}	video peak signal level	-	1.9	-	V
V_{TO-B}	video black signal level	-	1.0 - 2.0	-	V
V_{SYNC}	Y video sync pulse amplitude	-	0 - 4.0	-	V
Ro	Video output load	-	75	-	Ohm
t_H	horizontal line width		858		pclk
t_{HSYNC}	horizontal sync width		64		pclk
t_{HBK}	horizontal blank width		214		pclk
t_V	vertical field width		262.5		t_H
t_{VSYNC}	vertical sync width		3		t_H
t_{VF1}	field 1 vertical front equalization width		3		t_H
t_{VB1}	field 1 vertical back equalization width		3		t_H
t_{VBK1}	field 1 blank line outside equalization region		11		t_H
t_{VF2}	field 2 vertical front equalization width		3.5		t_H
t_{VB2}	field 2 vertical back equalization width		3		t_H
t_{VBK2}	field 2 blank line outside equalization region		11.5		t_H



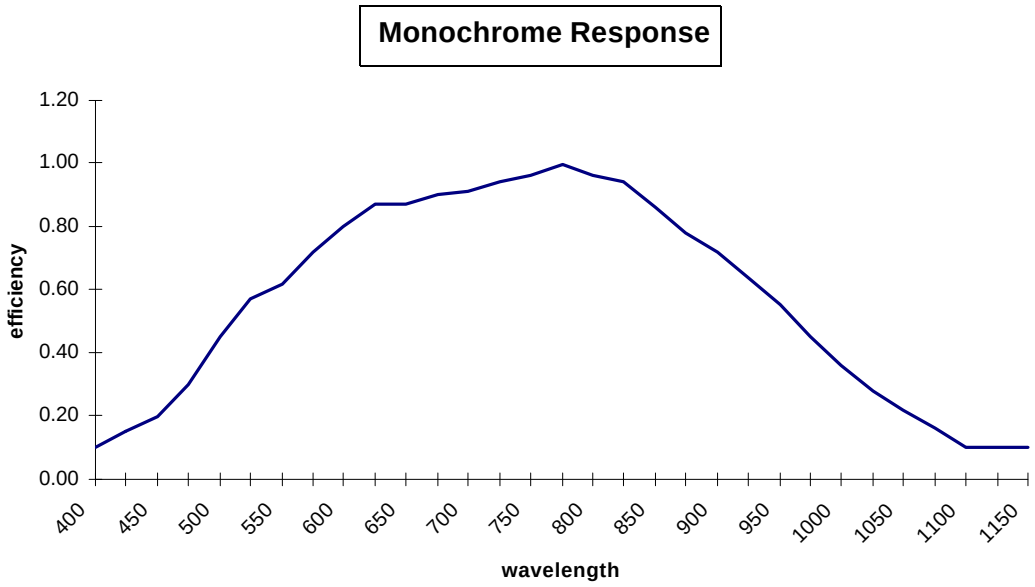


Figure 16. Spectrum Response

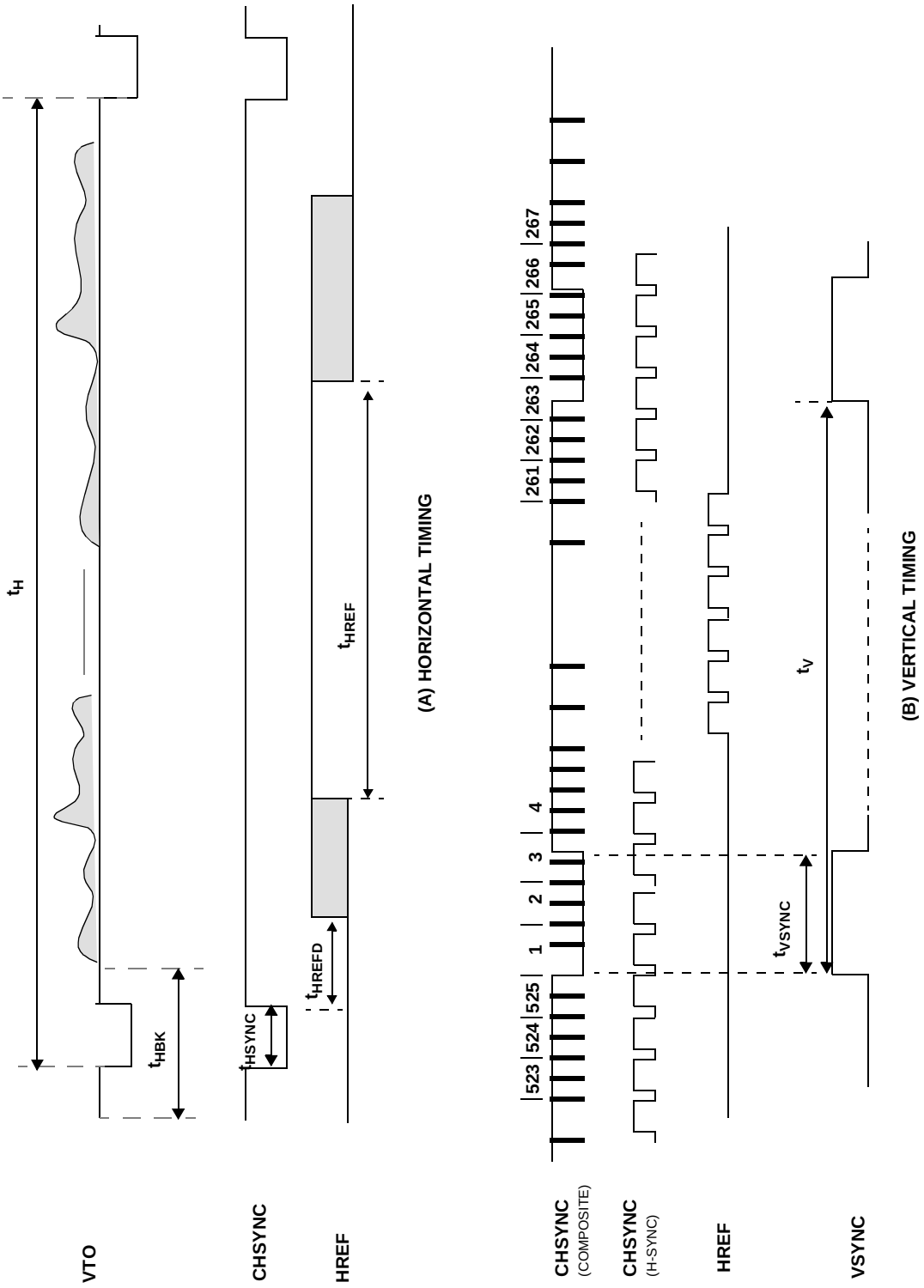


Figure 17. Video Timing Diagram

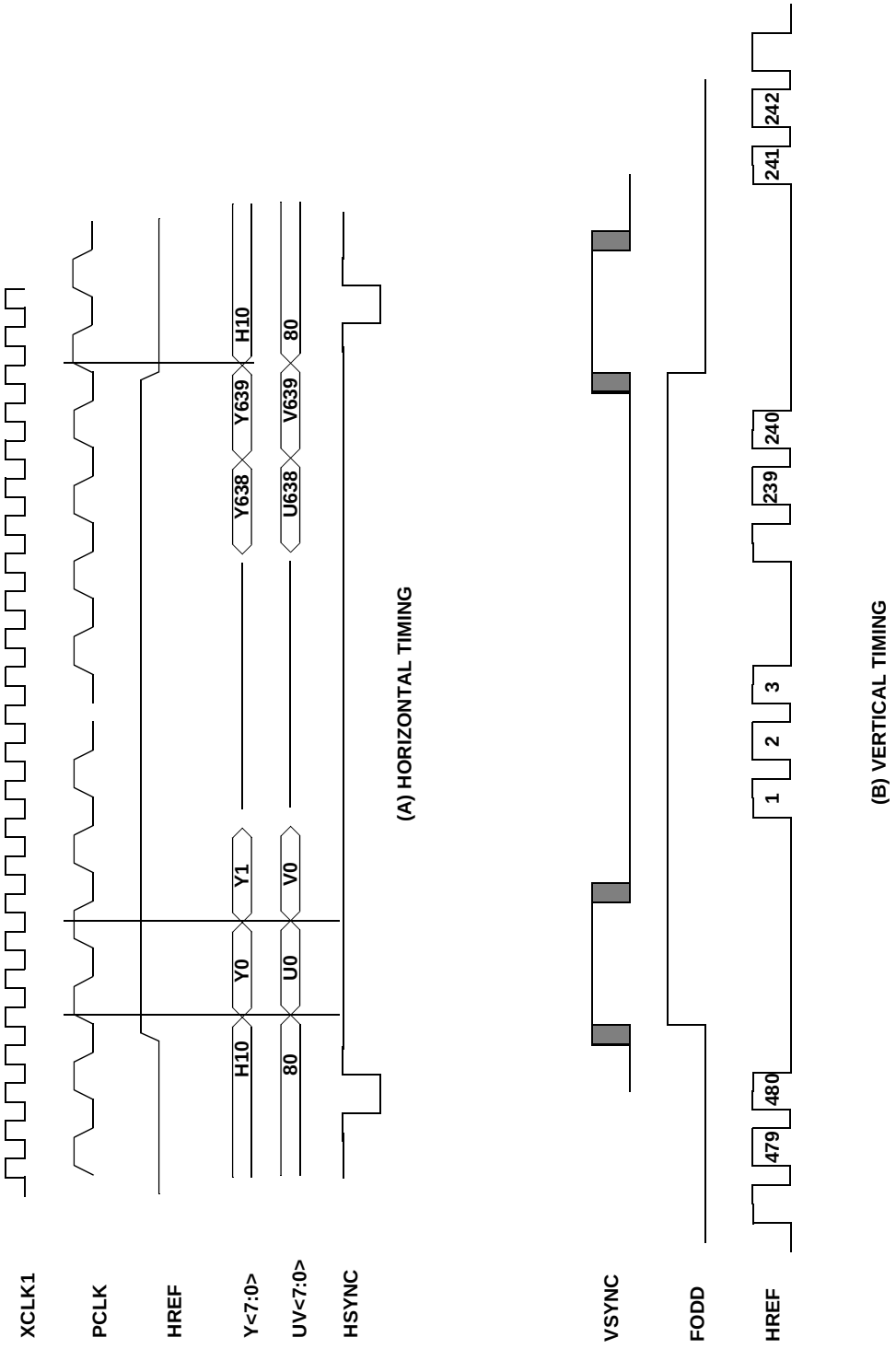


Figure 18. Digital Data Bus Timing

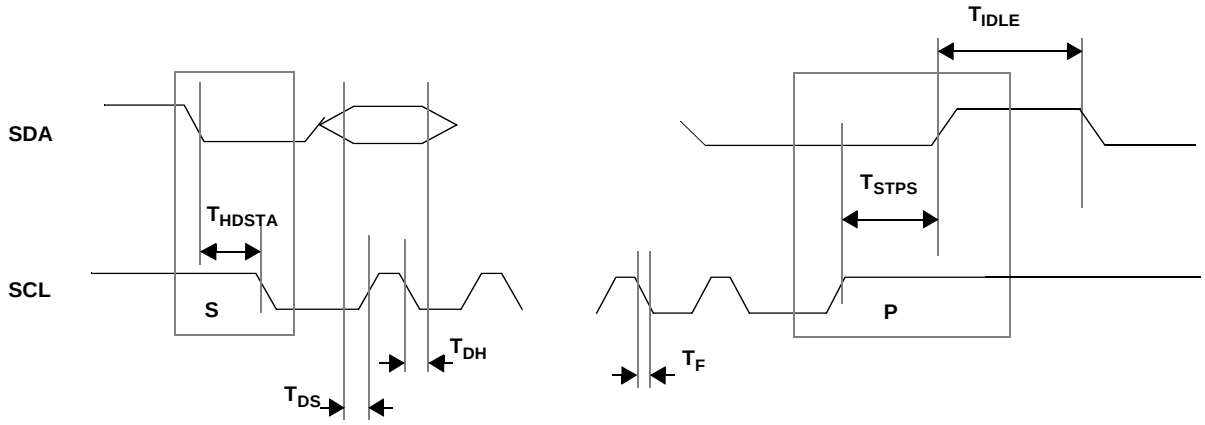


Figure 19. I²C Bus Timing

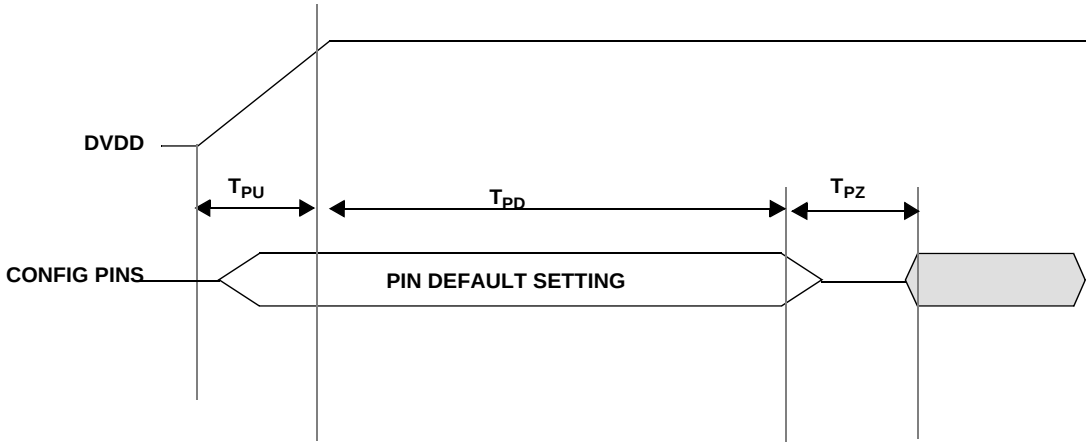


Figure 20. Configuration Pin Setting at Power Up

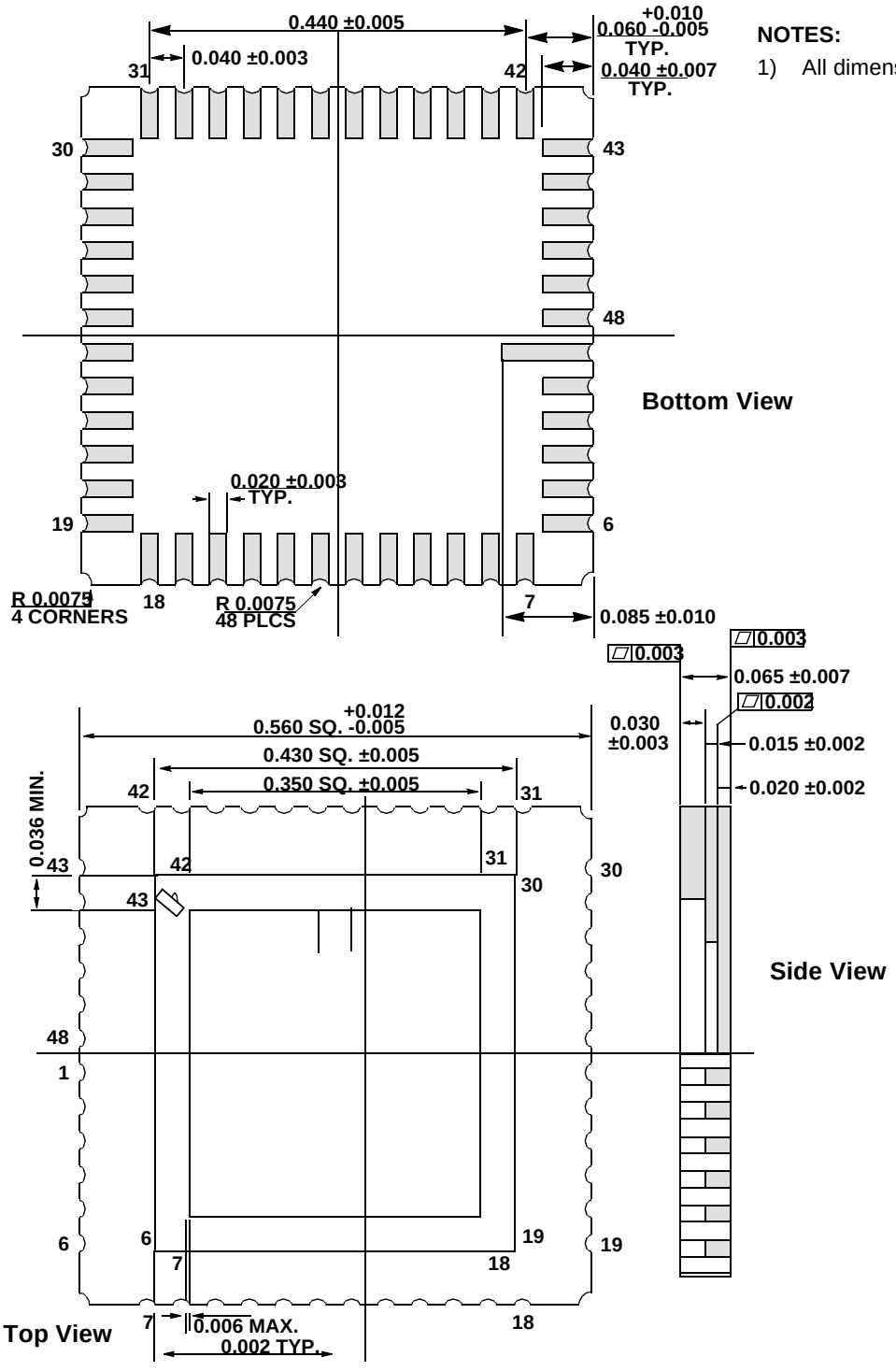
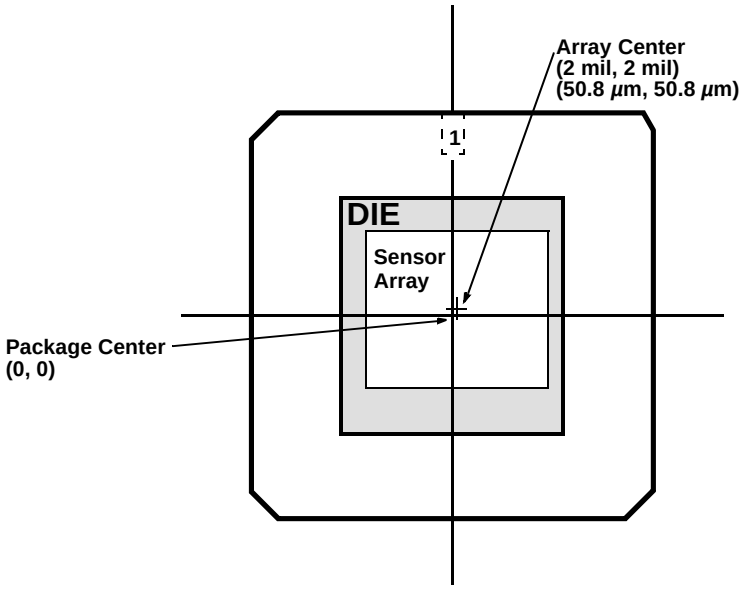


Figure 21. Package Mechanical Data

NOTES:

1) All dimensions in inches

.



Top View

Figure 22. OV7610/OV7110 Sensor Array Location

Part Number	Description	Comments
OV7610	Color Digital Sensor	48 pin LCC
OV7110	Monochrome Digital Sensor	48 pin LCC

Appendix

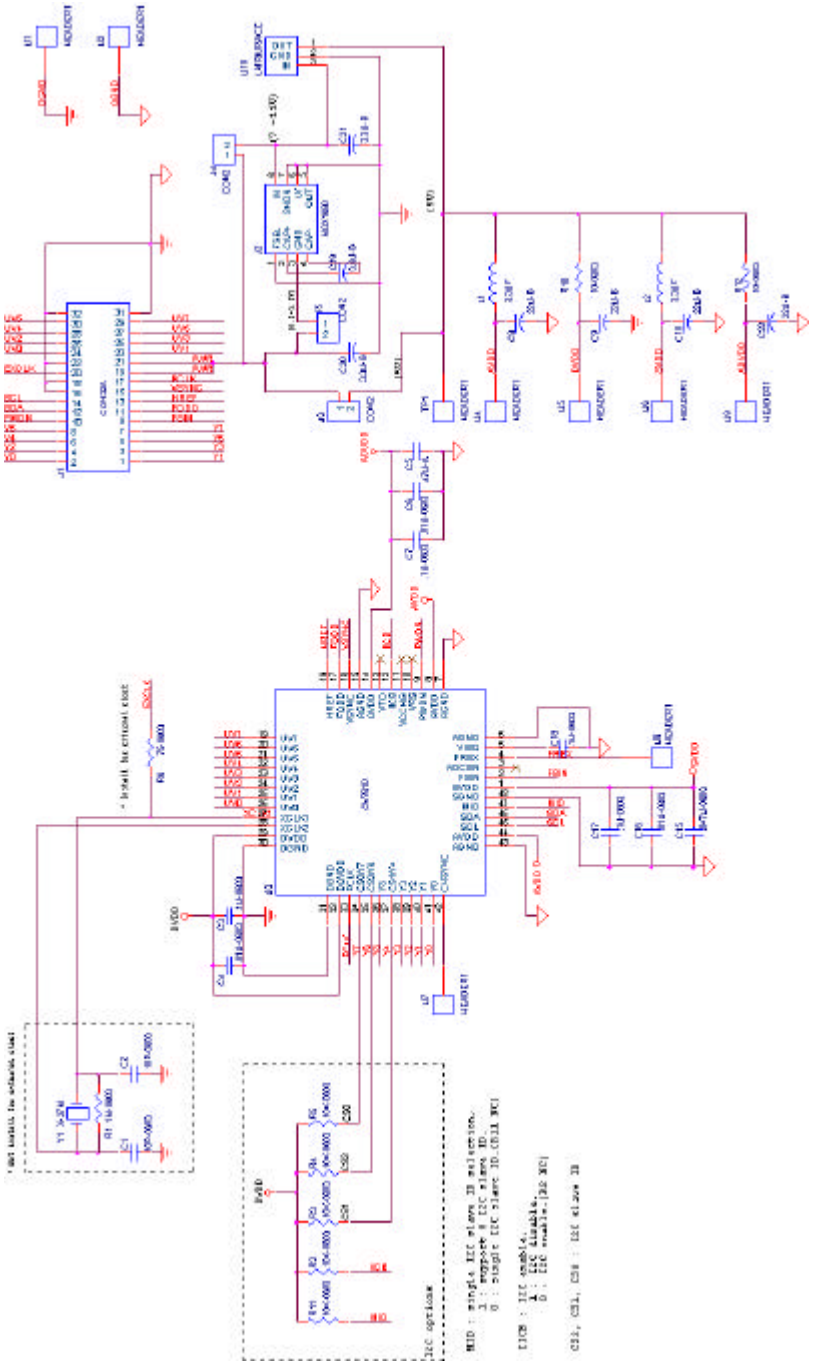
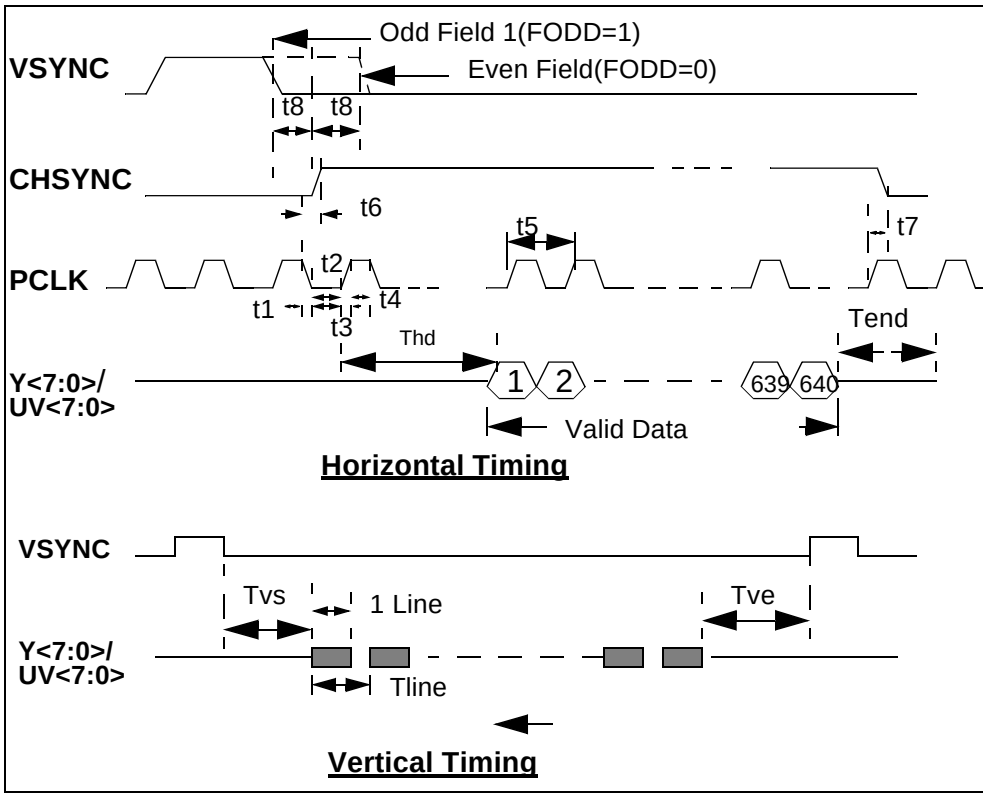


Figure 23. Referencing digital camera design

ZV PORT Timing:

The ZV Port is a single-source unidirectional video bus between a PC Card socket and a VGA controller. The ZV Port complies with CCIR601 timing to allow NTSC decoders to deliver real-time digital video straight into the VGA frame buffer from a PC Card. OV7600 support ZV Port Timing, which output signal can be output to a PC Card directly, then to VGA controller.ZV Port Timing



Notes: ZV Port format output signal include

VSYNC: Vertical sync pulse.

CHSYNC: Horizontal sync pulse.

PCLK: Pixel clock used to clock valid data and CHSYNC into ZV Port. Default frequency is 13.5MHz when use 27MHz as system clock. Rising edge of PCLK is used to clock the 16 Bit data.

Y<7:0>: 8 Bit luminance data bus.

UV<7:0>: 8 Bit chrominance data bus.

Note: In Interlaced Mode, there are Even/Odd field different (t8). When In Progressive Scan Mode, only frame timing same as Even field(t8).

:

Table A1: ZV Port AC Parameters

Symbol	Parameter	Min.	Max.
t1	PCLK fall timing	4 ns	8 ns
t2	PCLK low time	30 ns	
t3	PCLK rise time	4 ns	8 ns
t4	PCLK high time	30 ns	
t5	PCLK period	74 ns	
t6	Y/UV/CHSYNC setup time	10 ns	
t7	Y/UV/CHSYNC hold time	20 ns	
t8	VSYNC setup/hold time to CHSYNC	1 us	

Thd is the pixel number between 1st valid data and 1st **PCLK** rising after **CHSYNC** rising edge. When in default horizontal window setting, **Thd** = 142*t5, which is changed with register HS<7:0>. HS<7:0> increase 1, **Thd** increase 4 pixel clock.

Tend is the pixel number between last valid data and 1st **PCLK** rising edge after **CHSYNC** falling edge. When in default horizontal window setting, **Tend** = 10*t5, which is changed with register HE<7:0>. HE<7:0> change 1, **Tend** change 4 pixel clock.

After **VSYNC** falling edge, OV7600 will output black reference level, the line number is **Tvs**, which is the line number between the 1st **CHSYNC** rising edge after **VSYNC** falling edge and 1st valid data **CHSYNC** rising edge. Then valid data, then black reference, line number is **Tve**, which is the line number between last valid data **CHSYNC** rising edge and 1st **CHSYNC** rising edge after **VSYNC** rising edge. The black reference output line number is dependent on vertical window setting.

When in default setting, **Tvs** = 14***Tline**, which is changed with register VS<7:0>. If in **Interlaced Mode**, VS<7:0> change 1 step, **Tvs** increase 1 line. If in **Progressive Scan Mode**, VS<7:0> step equal to 2 line.

When in default setting, **Tve** = 4***Tline** for **Odd** Field, **Tve** = 3***Tline** for **Even** Field, which is changed with register VE<7:0>. If in **Interlaced Mode**, VE<7:0> change 1 step, **Tve** increase 1 line. If in **Progressive Scan Mode**, VE<7:0> step equal to 2 line.

In **Progressive Scan Mode**, **Tve** = 3***Tline** and **Tvs** = 35***Tline**.